

Phase & Frequency

Loop Mode

- maximum number of phases supported
- depending on which part number, there will be more or less combinations to select from

Operation Mode

- type of application
- POL/telecom is intended for ASIC and FPGA loads that does not follow Intel standards

Maximum (Nph)

- number of phases populated for the respective loop
- value mostly depends on the full load current rating of the application and current capability per phase
- the controller uses the Nph value to set the internal phase timing relationship for the loop
- for normal applications, **Maximum = PS0 State**

Fsw

- switching frequency
- depending on NPH in a loop, available frequencies may differ slightly due to internal division ratios

Use Doubler Driver

- enable to use 2 power stages per phase in doubler configuration. Causes the PWM frequency at the PWM pin to double as the driver will divide the PWM again.

Phase and Frequency - 0x6C

Loop Mode: 7 + 1

Operation Mode: Intel

☒ Enable Auto Phase Detect

Pinout Diagram

Loop A

Number of Phases (Nph)

Maximum: 7

PS0 State: 7

PS1 State: 1

PS2 State: 1

PS3 State: 1

Fsw: 714 kHz

Max Duty Cycle: 56.25 %

☐ Use Doubler Driver

Loop B

Number of Phases (Nph)

Maximum: 1

PS0 State: 1

PS1 State: 1

PS2 State: 1

PS3 State: 1

Fsw: 521 kHz

Max Duty Cycle: 56.25 %

☐ Use Doubler Driver

Write to device Read from device Close Help

Enable Auto Phase Detect

- automatic detection of number of mounted phases on a board
- recommended to always have box marked

Pinout Diagram

- displays pinout diagram of the device

PSx State

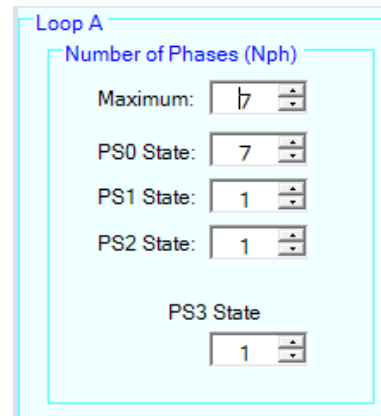
- number of phases enabled during specific power states
- Should be set based on load current requirement for the system and current capability per phase. This is usually limited by the power device used.
- Maximum >= PS0 >= PS1 >= PS2 >= PS3**
- For normal applications, **PS0 State = Maximum**
- if not used, set all **PSx State = Maximum** phases
- typically used for Intel applications
- for AMD, see note on next page

Max Duty Cycle

- Maximum duty cycle allowed for PWM signal
- calculate for minimum Vin and Max Vout operation
- May need to be higher (50% or more often used) to allow for transient condition during steps in load

Phase & Frequency

- › For AMD, the power states translate to
 - PS0 State=normal operation
 - PS1 State=PSI0_L
 - PS2 State=PSI1_L
 - PS3 State= Not Used (set to same as PS2)



The screenshot shows a configuration window titled 'Loop A'. Inside, there is a section 'Number of Phases (Nph)' with a 'Maximum' value of 7. Below this, there are four power state settings, each with a numeric input field and a dropdown arrow:

- PS0 State: 7
- PS1 State: 1
- PS2 State: 1
- PS3 State: 1

Note: GUI does not change the text for different modes like AMD. It always uses the Intel names.